Flip-chip Interconnection between Nb_5N_6 Terahertz Array Detectors and Readout Circuits

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Abstract—Nb_5N_6 microbolometer is a high sensitive terahertz detector at room temperature, but its integrated air cavity structure increases the difficulty of interconnection with readout circuit. For this reason, we optimized the flip chip process and successfully realized the interconnection between 32 × 32 array devices and readout circuits.

I. Introduction

$b_5N_6$microbolometer is a high sensitive terahertz (THz) detector which works at room temperature and is easy to be integrated on a large scale[1]. We further optimized the flip chip bonding process [2] to avoid the influence of mechanical and thermal factors on the integrated air cavity structure and film of the device, and successfully realized the interconnection between array devices and the readout circuit.

II. Results

Firstly, we designed and prepared 32×32 Nb_5N_6 microbolometer arrays and each pixel size is 250 μm×250 μm. The core of the each pixel is a 3 μm×12 μm Nb_5N_6 microbridge integrated with air cavity and double slot antenna [3]. The antennas and electrodes are made of a *UBM* (Under Bump Metallization) layer (the thickness of UBM layer is Ti/Au/Pt/Au=20nm/120 nm/30 nm/120nm respectively). The optical image of the 32×32 Nb_5N_6 microbolometer arrays device is shown in Fig.1. The 0.18 μm CMOS process is applied to the readout circuit array.

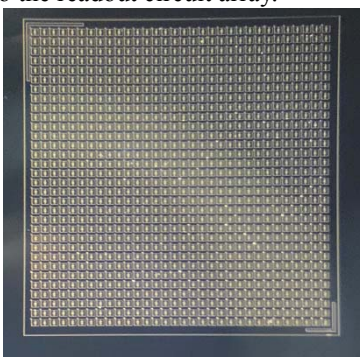
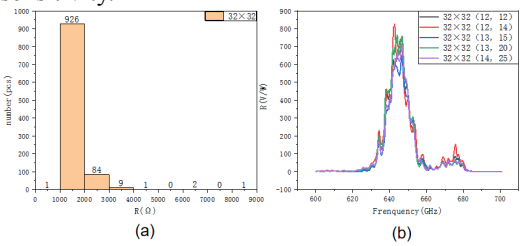


Fig.1. the optical image 32×32 Nb_5N_6 microbolometer arrays device

We evaluate the uniformity of the device by measuring the resistance distribution of each pixel with a probe stage (MPI TS2000-SE). Statistics of the distribution of all the resistance values are shown in fig.2 (a). It shows that more than 90% of the resistance values are distributed in the range of 1 kΩ~2 kΩ. The DC responsivity of the device is obtained by I-V measurement, the optimal bias current of the device is near 0.2 mA, and the DC responsivity is distributed in 500V/W~600V/W. The optical response of the device is also characterized, and Fig.2 (b) shows the RF response of five randomly selected pixels. The results show that in the response range of 640 GHz~660 GHz, the RF voltage responsivity is all about 700V/W. The above results suggest that the array device has good consistency and high sensitivity.



(a) (b)

Fig.2. (a)Resistance distribution of the 32×32Nb_5N_6 microbolometer arrays. (b)DC responsivity of the 32×32Nb_5N_6 microbolometer arrays.

Then indium solder bumps are grown on the electrodes of the devices by photolithography and lift-off. The diameter and height of solder bumps are 18 μm and 6 μm respectively. The same *UBM* layer and solder bumps are also grown on the electrodes of the readout circuit. Finally, the device and the circuit are connected by alignment and cold pressing. In order to improve the firmness, glue is filled into the outside of the two parts. The process is shown in fig.3.

The 3D image of indium solder bumps of the device measured by white light interferometer is shown in Fig.4 (a). It reveals that solder bumps are very uniform, and the height is consistent with the design value. Fig.4(b) is an optical micrograph of the device and the circuit during flip-chip process. The final interconnected chip is shown in Fig.4(c). The preliminary measure results show that the interconnection is successful. Later, we will use the imaging system to further characterize the chip performance.

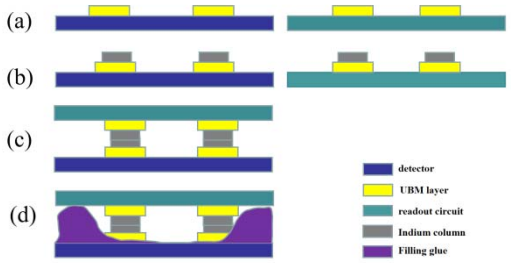


Fig. 3. (a) Grow a layer of *UBM* on the device and readout circuit chip respectively. (b) Grow an indium solder bump on the electrodes (c) Connect by cold pressure welding (d) Fill the gap of the connection with glue.

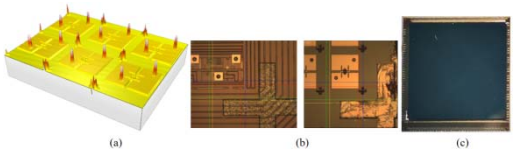


Fig.4. (a) A 3D image of indium solder bumps of the device (b) Optical micrographs of the device and the circuit during flip-chip process (c) A image of final interconnected chip.

III. SUMMARY

We successfully fabricate 32×32 Nb_5N_6 terahertz detector array, and realize the interconnection between detector and the readout circuit through the flip-chip process. The interconnected chip will be further tested and characterized later.

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