Design of Superconducting Terahertz Digicam

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***Abstract*—We have made cold readout electronics with GaAs-JFETs for submillimeter-wave SIS photon detector arrays. The readout electronics consists of 4-channel charge integrating amplifier, multiplexers and digital electronics. We are going to present the performance of the cryogenic readout electronics and design of superconducting terahertz digital camera with the SIS photon detectors.**

I. Introduction

We have been working on superconducting direct detectors with niobium tunnel junctions, the submillimeter-wave SIS photon detectors[1]. The detectors have high dynamic range and fast response and also operate at higher temperature than bolometric detectors. Those detectors are suitable for wide range of applications including astronomy and high dynamic range and short exposure terahertz imaging. Cryogenic readout electronics are now being developed to realize large format array of SIS photon detectors to apply to various applications.

The readout electronics consists of cryogenic integrating amplifiers with low noise and low power dissipation using SONY GaAs-JFETs. Based on the DC characteristics of GaAs-JFETs and single stage amplifiers, we have designed high gain amplifiers. Small scale integrated circuits have been fabricated including analog and digital circuits.

II. Cryogenics electronics

The analog amplifier is based on capacitive trans-impedance amplifiers with the gain of more than 2000. Power dissipation is designed to be less than 4 μW/ch and input referred noise of about $1\mu W/Hz^{0.5}$ at 1 Hz. To cancel input offset voltage of GaAs-JFETs, integrating amplifier is AC-coupled and DC voltage is applied to the detectors from external circuit. For stable operation of the feedback circuits, on-chip compensation capacitors are used. Upper part of the Fig. 1 shows the image of 4-channel CTIA circuit.

Multiplexing circuit consists of sample-and-hold circuits, multiplexer circuit that can be addressed by shift registers operated at the same cryogenic temperature. To confirm operation of cryogenic digital circuit, basic circuit such as NAND and NOR is tested and their operation was measured as expected. Lower part of the Fig. 1 shows the two sets of 4-channel shift registers based on Direct Coupled FET Logic (DCFL) that uses depletion and enhancement type GaAs-JFETs with power dissipation of only 0.5μW/ch.

Using these circuits, we are going to demonstrate 32-channel imaging array of SIS photon detector, which can be named as the superconducting terahertz digital camera. The design details of the camera will be discussed at the meeting.

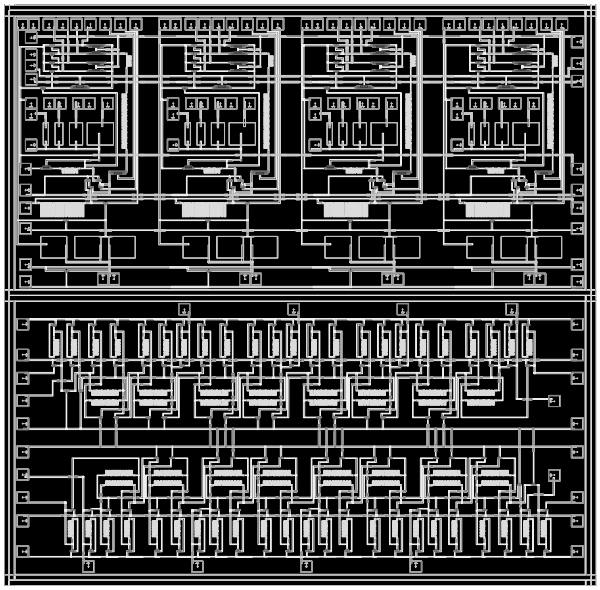

Figure 1. A CAD drawing of 4-channel CTIA circuits and two 4-channel shift registers integrated on a 3.8 mm x 3.8 mm GaAs chip.

References

[1] Matsuo, H., Mori, Y., Murakoshi, Y., Ariyoshi, S., Ezawa, H., Hibi, Y., Kobayashi, J., Nagata, H., Nakahashi, M., Otani, C., "Realization of submillimeter-wave imaging array with superconducting direct detectors", 2008, J. Low Temp. Phys. 151, 304-309.

[2] Nagata, H., Kobayashi, J., Matsuo, H., Nakahashi, M., Kobayashi, K., Ikeda, H., Fujiwara, M., "Fabrication of cryogenic readout circuits with n-type GaAs-JFETs for low temperature detectors", 2008, J. Low Temp. Phys. 151, 1022-1027

[3] S. Ariyoshi, C. Otani, A. Dobroiu, H. Sato, K. Kawase, H. M. Shimizu, T. Taino, H. Matsuo, "Terahertz imaging with a direct detector based on superconducting tunnel junctions", 2006, *Appl. Phy. Lett.* 88, 203503.

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