Low-loss porous silicon substrates for microwave and millimeter applications

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***Abstract*—This paper propose the utilization of a photolithographic process to elevate the metal lines position that relative to the wafer plane, in order to take advantage from the signal propagation practically on-the-air, gained an almost ideal TEM mode of propagation in CPW structure. S-parameter and coupling degree of CPW with Porous Si (PS), SOI and high resistivity Silicon (HRS)、SOI substrates are compared.**

I. Introduction And Background

As communication systems are increasingly moving to millimeter wave frequencies it is now theoretically possible to have most of the transceiver implemented on a single CMOS chip. CMOS is a standard and low cost process becoming more commonly used for RFIC and microwave and millimeter applications. Unfortunately designs have mostly avoided fabricating passive on-chip passive components on standard CMOS technology because of the loss nature of the silicon substrate poor performance and stringent foundry fabrication design rules [1-2]. Highly stable and mechanically strong thick porous silicon (PS) films could be obtained on textured silicon substrates which exhibits higher porosity, better mechanical strength, non-fractured surface morphology and lower stress. Porous silicon with more than 50% porosity has low loss tangent (below 10^{-3}) at 20 GHz [3-5].

II. Results

Firstly, thick porous Si layers has been fabricated on the low resistivity silicon substrate without severe stress, moreover, the leakage currents between the ground planes and the central conductor of the CPW line are lowered. Relative dielectric constants of porous silicon are adjustable from 3 to 9 by changing porosity of PS from 80% to 25%. The post-treat thick porous silicon layer as the cathode is applied about 10mA/cm^2 current in mixture of ethanol, HF and H_2O_2 solutions improved stability, surface smoothness and mechanical property of the PS layers. Then, the polyimide is coated on PS by means of spinning process; spinning speed depends on polyimide thickness (Fig.1).

Secondly, the gap between ground and signal line will cause field leakage and radiation loss which will result in different inter-layer parasitic coupling. Finite ground CPW is used to inhibit the cross-interference and parasitic coupling. The exploited CPW structure is shown in Fig2. Fig.3.is the coupling line model and its equivalent circuit of the coupling line considering the substrate.

A. Study of CPW on different substrate

Figs.4 is magnitude of the electromagnetic field by simulations the CPW lines with polyimide (a) and without polyimide (b). It is obvious that the biggest part of electric field from 3.228e+005 V/m decreases to 3.1543 e+005V/m, because of the spin-coated polyimide. The spin-coated polyimide layer changes the energy of the air above the substrate and the metal line. So the energy losing in the PS substrate and directly lead to the decrease of the whole loss. At high frequency, substrate loss of PS with spin-coated polyimide is less than that of the HRS and very near quartz (QUA) substrate (Fig.5), which could be easily explained by the simulated electric field distribution. Fig.6 shows simulated and measured structure on polyimide / PS substrate.

B. Study of coupling degree on different substrate

Fig.7. is comparison among three different materials' coupling degree. Under high frequency (greater than 20GHz), the coupled degree of PS is -35.71dB, HRS and SOI substrate is -31.64dB and -32.47dB respectively. It proves that the coupling of PS substrate with spin-coated polyimide is excellent.

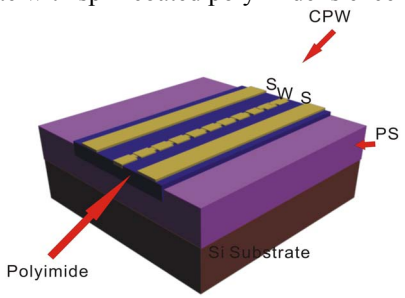

Fig.1. CPW structures on Porous Silicon (PS) with thin polyimide

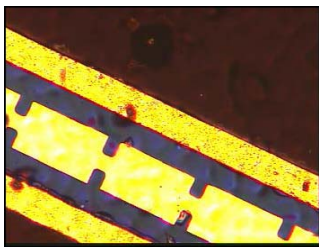

Fig.2. CPW lines on polyimide/PS substrates

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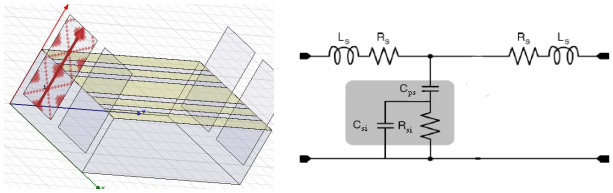
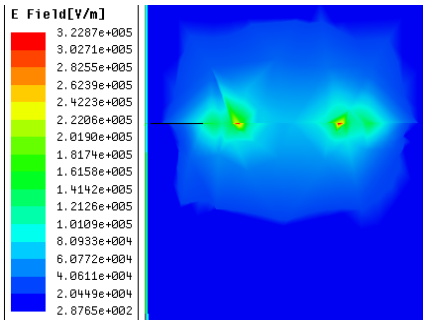
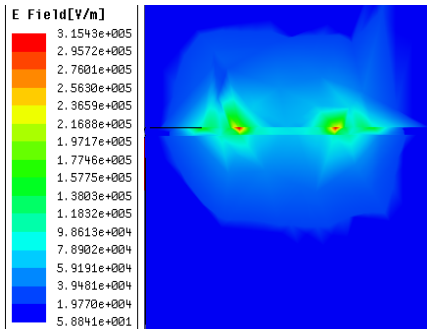


Fig.3.Coupling line model and its equivalent circuit



(a)



(b)

Fig.4. electromagnetic field

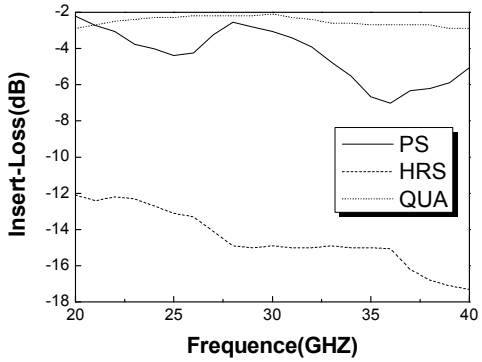


Fig.5. Insert loss of different substrates

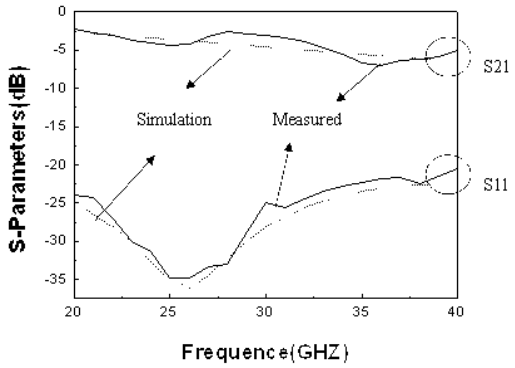


Fig.6.Simulated and experimental response of the CPW on PS substrate

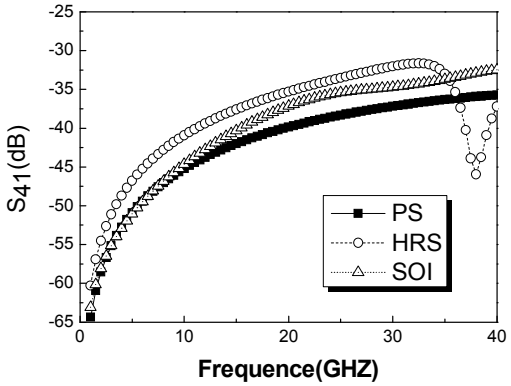


Fig.7. Coupled degree of three substrates

ACKNOLEDGMENT

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